

	Document ID	Issue Date	Pages	Title	Current OR	Inventor
15	US 6867607 B2	20050315	8	Membrane test method and apparatus for integrated circuit testing	324/754	Degani; Yinon et al.
16	US 6861864 B2	20050301	14	Self-timed reliability and yield vehicle array	324/765	Schultz; Richard
17	US 6836014 B2	20041228	14	Optical testing of integrated circuits with temperature control	257/706	Hunt; Dean M. et al.
18	US 6795800 B1	20040921	12	Simplified method for extracting model parameter sets and method for statistically simulating integrated circuit using the same	703/2	Lee; Sang-hoon
19	US 6539526 B1	20030325	15	Method and apparatus for determining capacitances for a device within an integrated circuit	716/5	Deng; Xiaowei
20	US 6452198 B1	20020917	16	Minimized contamination of semiconductor wafers within an implantation system	250/492.21	Mani; Balaraman et al.
21	US 6251706 B1	20010626	18	Method for cooling the backside of a semiconductor device using an infrared transparent heat slug	438/122	Paniccia; Mario J.
22	US 6244874 B1	20010612	6	Electrical contactor for testing integrated circuit devices	439/66	Tan; Yin Leong
23	US 6221682 B1	20010424	14	Method and apparatus for evaluating a known good die using both wire bond and flip-chip interconnects	438/15	Danziger; Steve M et al.
24	US 6168311 B1	20010102	16	System and method for optically determining the temperature of a test object	374/161	Xiao; Guoqing et al.
25	US 5895972 A	19990420	19	Method and apparatus for cooling the backside of a semiconductor device using an infrared transparent heat slug	257/706	Paniccia; Mario J.
26	US 5717369 A	19980210	37	Array oscillator circuit	331/57	Maneatis; John George et al.
27	US 5475344 A	19951212	36	Multiple interconnected ring oscillator circuit	331/57	Maneatis; John G. et al.
28	US 4841134 A	19890620	34	IC card	235/488	Hida; Yoshiaki et al.

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1	US 20060023564 A1	20060202	30	Signal output device and method for the same	365/233	Kanzaki; Hideyuki et al.
2	US 20050188212 A1	20050804	8	Optical testing of integrated circuits with temperature control	324/158.1	Hunt, Dean M. et al.
3	US 20050088194 A1	20050428	8	Testing integrated circuits	324/754	Degani, Yinon et al.
4	US 20050015651 A1	20050820	20	Self-timed reliability and yield vehicle with gated data and clock	714/5	Schultz, Richard et al.
5	US 20040207406 A1	20041021	15	Self-timed reliability and yield vehicle array	324/535	Schultz, Richard
6	US 20040188868 A1	20040610	15	Device speed alteration by electron-hole pair injection and device heating	324/765	Eiles, Travis et al.
7	US 20040058880 A1	20040408	9	Optical testing of integrated circuits with temperature control	257/48	Hunt, Dean M. et al.
8	US 20030144860 A1	20030731	14	AUTOMATIC INTEGRATED CIRCUIT TESTING SYSTEM AND DEVICE USING AN INTEGRATIVE COMPUTER AND METHOD FOR THE SAME	324/158.1	CHI, MING-REN et al.
9	US 20030127315 A1	20030724	9	Testing integrated circuits	324/754	Degani, Yinon et al.
10	US 20010831508 A1	20011018	14	Method and apparatus for evaluating a known good die using both wire bond and flip-chip interconnects	438/17	Danziger, Steve M. et al.
11	US 7061258 B2	20060613	8	Testing integrated circuits	324/754	Degani, Yinon et al.
12	US 6914424 B2	20050705	13	Automatic integrated circuit testing system and device using an integrative computer and method for the same	324/158.1	Chi, Ming-Ren et al.
13	US 6900654 B2	20050531	13	Method and apparatus for evaluating a known good die using both wire bond and flip-chip interconnects	324/765	Danziger, Steve M et al.
14	US 6882170 B2	20050419	13	Device speed alteration by electron-hole pair injection and device heating	324/765	Eiles, Travis et al.

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1	US 20030173990 A1	20030918	15	Wafer map display apparatus and method for semiconductor test system	324/765	Nanbu, Mitsue
2	US 6774620 B2	20040810	15	Wafer map display apparatus and method for semiconductor test system for displaying an image of wafer and IC chips with optimum display size	324/158.1	Nanbu; Mitsue
3	US 6552527 B1	20030422	10	Wafer map display apparatus and method for semiconductor test system	324/158.1	Nanbu; Mitsue
4	US 6246248 B1	20010612	10	Tester for detecting an abnormal quiescent power supply current in a device under test	324/763	Yamagishi; Masaru
5	US 5640539 A	19970617	23	IC analysis system having charged particle beam apparatus for improved contrast image	716/21	Goishi; Akira et al.
6	US 5319353 A	19940607	26	Alarm display system for automatic test handler	340/525	Ohnishi; Takeshi et al.
7	US 5247468 A	19930921	14	System for calculating and displaying user-defined output parameters describing behavior of subcircuits of a simulated circuit	703/14	Henrichs; Dale K. et al.
8	US 3657527 A	19720418	17	SYSTEM FOR AUTOMATICALLY CHECKING BOARDS BEARING INTEGRATED CIRCUITS	714/736	Kassabgi; Georges et al.

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1	US 20050168212 A1	20050804	8	Optical testing of integrated circuits with temperature control	324/158.1	Hunt, Dean M. et al.
2	US 20040065880 A1	20040408	9	Optical testing of integrated circuits with temperature control	257/48	Hunt, Dean M. et al.
3	US 6836014 B2 X	20041228	14	Optical testing of integrated circuits with temperature control	257/706	Hunt; Dean M. et al.
	US 6795800 B1	20040921	12	Simplified method for extracting model parameter sets and method for statistically simulating integrated circuit using the same	703/2	Lee; Sang-hoon
5	US 6251706/B1 X	20010626	18	Method for cooling the backside of a semiconductor device using an infrared transparent heat slug	438/122	Paniccia; Mario J.
6	US 5895972 A X	19990420	19	Method and apparatus for cooling the backside of a semiconductor device using an infrared transparent heat slug	257/706	Paniccia; Mario J.

	L #	Hits	Search Text	DBs
3	L3	474151	(ic or integrated adj circuit\$4)	US- PGPUB; USPAT
4	L4	3694	evaluat\$3 with (ic or integrated adj circuit\$4)	US- PGPUB; USPAT
5	L5	1573	L4 and (evaluat\$3 near\$3 (ic or integrated adj circuit\$4))	US- PGPUB; USPAT
6	L6	1109	L5 and (evaluat\$3 near\$2 (ic or integrated adj circuit\$4))	US- PGPUB; USPAT
7	L7	477	L6 and (evaluat\$3 near\$1 (ic or integrated adj circuit\$4))	US- PGPUB; USPAT
8	L8	281	L6 and (evaluat\$3 adj\$1 (ic or integrated adj circuit\$4))	US- PGPUB; USPAT
9	L9	28	L8 and ((evaluat\$3 adj\$1 (ic or integrated adj circuit\$4)) with (variable\$1 or parameter\$1 or performance))	US- PGPUB; USPAT
10	L10	6	L8 and ((evaluat\$3 adj\$1 (ic or integrated adj circuit\$4)) with (variable\$1 or parameter\$1))	US- PGPUB; USPAT
11	L12	1	L11 and (gui or graphic\$4 or diagram\$1)	US- PGPUB; USPAT
12	L11	1	"6795800".pn.	US- PGPUB; USPAT
13	L13	17	L8 and (display\$3 with result\$3)	US- PGPUB; USPAT
14	L15	6	L14 and compar\$4	US- PGPUB; USPAT

	L #	Hits	Search Text	DBs
15	L16	2	L15 and graphic\$2	US- PGPUB; USPAT
16	L14	8	L13 and (display\$3 near3 result\$3)	US- PGPUB; USPAT